FEATURES

- Input voltage range: 3V to 40V
- Ultra-low quiescent current <6μA
- Low dropout voltage: 200mV @ 100mA
- Maximum output current: 300mA Ultra-low power sleep mode
- Shutdown current <1μA
- High PSRR 60dB @ 100Hz
- Stable with low-ESR ceramic output-stability capacitor (2.2 μF)
- Enable Pin (EN) withstand voltage: 40V
- Overcurrent protection, short-circuit protection
- Virtual junction temperature range: -40℃ to 150℃
- Thermal shutdown and automatic restart recovery
- Built-in soft start
- Support ESOP8, EMSOP8 and SOT89-5 packages

PRODUCT APPEARANCE

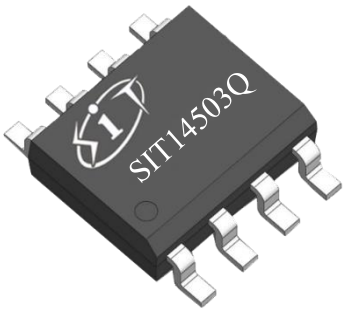


Fig 1 provides green, lead-free packaging

DESCRIPTION

The SIT14503Q series is a low dropout linear regulator (LDO) with ultra-low quiescent current and a wide input voltage range of 3V to 40V. SIT14503Q provides fixed output of 5V. In addition, the product family is available with fixed outputs of 2.5V, 3.3V and 15V, or adjustable outputs from 0.65V to 24V [(1)], providing load currents up to 300mA. The quiescent current of the SIT14503Q series is less than 1μA when disabled and less than 6μA at light loads. The power-good delay can be adjusted by external components, allowing the delay time to be configured to fit application-specific systems. It can be applied to the power management of automotive electronics, industrial control system and wide voltage battery power supply system.

NOTE [(1)]: If you need any other versions of the SIT14503Q series except for the fixed 5V output, please contact the sales.

PIN CONFIGURATION

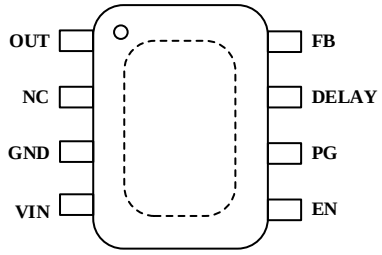


Fig 2 ESOP8 package pin configuration

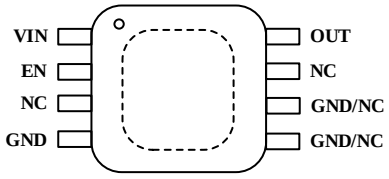


Fig 3 EMSOP8 package pin configuration

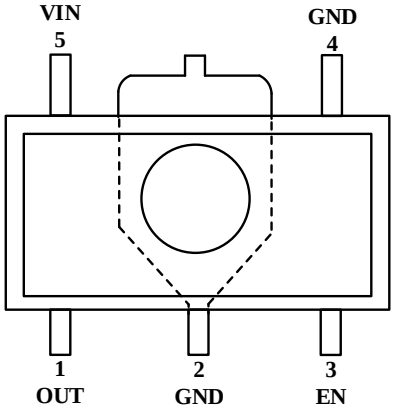


Fig 4 SOT89-5 package pin configuration

PIN DESCRIPTION

Table 1 ESOP8 package pin description

Pin	Symbol	Pin description
1	OUT	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, use a 2.2-µF or larger ceramic capacitor from OUT to GND.
2	NC	NC pin. This pin can either be left floating or connected to GND.
3	GND	Ground pin. Connect this pin to the thermal pad with a low-impedance connection.
4	VIN	Input power-supply voltage pin. For best transient response and to minimize input impedance, place a 1-µF or larger ceramic capacitor between the VIN and GND.
5	EN	Enable pin. The device is disabled when the enable pin becomes lower than the enable logic input low level (V_{IL}). Do not leave this pin floating because this pin is high impedance. If left floating, this pin

Pin	Symbol	Pin description
		may cause the device to enable or disable.
6	PG	Power-good pin. Power-good pin. This pin has an internal pullup resistor. Do not connect this pin to V_{OUT} or any other biased voltage rail. V_{PG} is logic level high when V_{OUT} is above the power-good threshold.
7	DELAY	Power-good delay adjustment pin. Connect a capacitor from this pin to GND to set the PG reset delay
8	FB	This pin is a feedback pin when using an external resistor divider. When using the adjustable device, this pin must be connected through a resistor divider to the output for the device to function.

Table 2 EMSOP8 package pin description

Pin	Symbol	Pin description
1	VIN	Input power-supply voltage pin. For best transient response and to minimize input impedance, place a 1-μF or larger ceramic capacitor between the VIN and GND.
2	EN	Enable pin. The device is disabled when the enable pin becomes lower than the enable logic input low level (V_{IL}). Do not leave this pin floating because this pin is high impedance. If left floating, this pin may cause the device to enable or disable.
3	NC	NC pin. This pin can either be left floating or connected to GND.
4	GND	Ground pin. Connect this pin to the thermal pad with a low-impedance connection.
5	GND/NC	Ground pin. Connect this pin to the thermal pad with a low-impedance connection or not connected.
6	GND/NC	Ground pin. Connect this pin to the thermal pad with a low-impedance connection or not connected.
7	NC	NC pin. This pin can either be left floating or connected to GND.
8	OUT	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, use a 2.2-μF or larger ceramic capacitor from OUT to GND.

Table 3 SOT89-5 package pin definition

Pin	Symbol	Pin description
1	OUT	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, use a 2.2-μF or larger ceramic capacitor from OUT to GND.

Pin	Symbol	Pin description
2	GND	Ground pin. Connect this pin to the thermal pad with a low-impedance connection.
3	EN	Enable pin. The device is disabled when the enable pin becomes lower than the enable logic input low level (V_{IL}). Do not leave this pin floating because this pin is high impedance. If left floating, this pin may cause the device to enable or disable.
4	GND	Ground pin. Connect this pin to the thermal pad with a low-impedance connection.
5	VIN	Input power-supply voltage pin. For best transient response and to minimize input impedance, place a 1μF or larger ceramic capacitor between the VIN and GND.

Note: for all packages, it is recommended that the thermal pad is soldered to board ground.

FUNCTIONAL BLOCK DIAGRAM

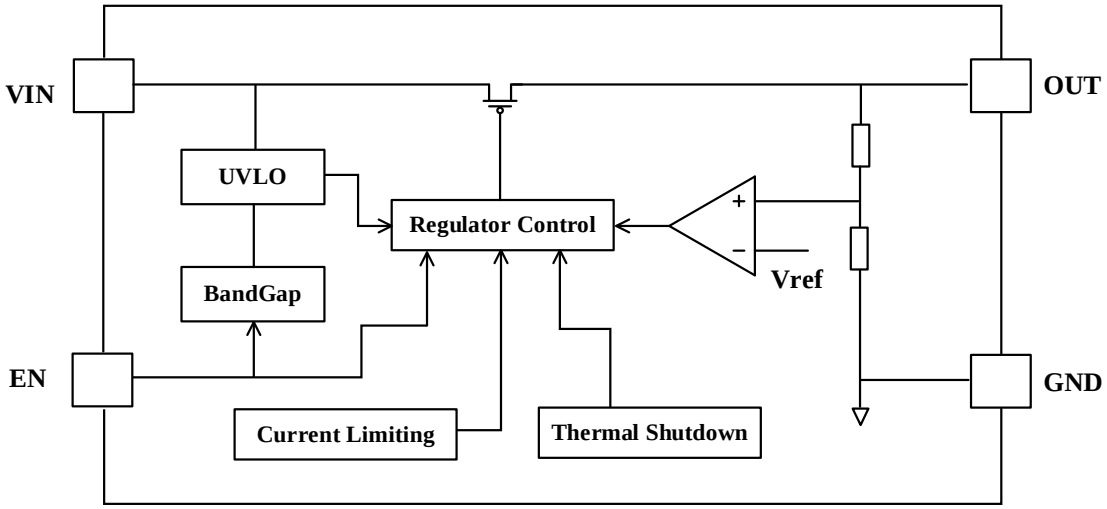


Fig 7 Internal block diagram of SIT14503Q fixed output series

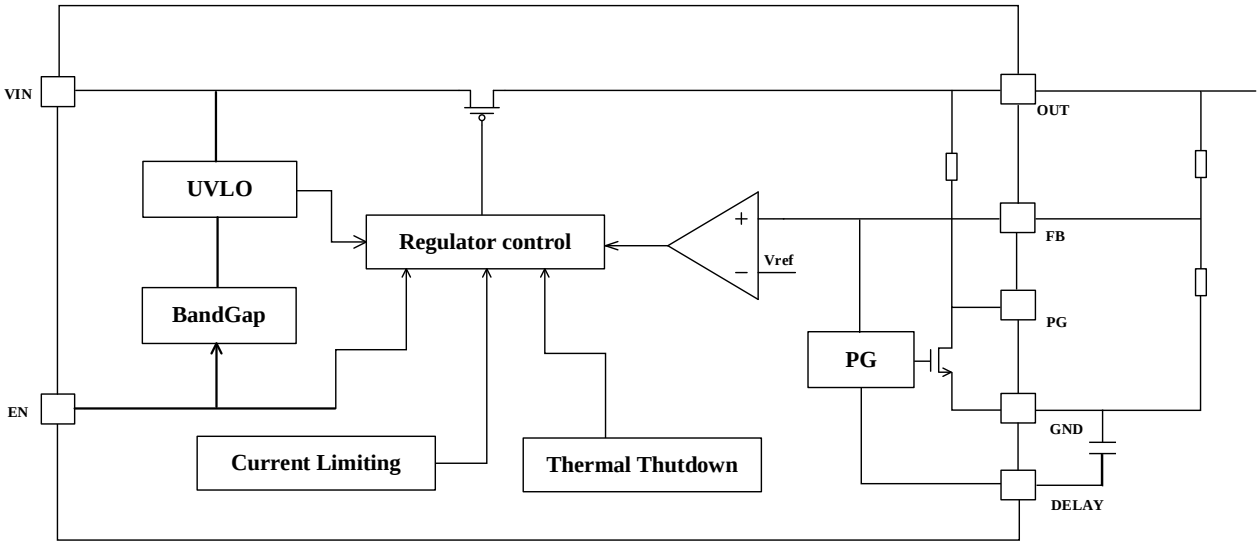


Fig 8 Internal block diagram of SIT14503Q adjustable output series

FEATURE DESCRIPTION

1 Overview

The SIT14503Q series is a low dropout linear regulator (LDO) with ultra-low quiescent current and a wide input voltage range of 3V to 40V. The quiescent current of the SIT14503Q series is less than 1μA when disabled and less than 6μA at light loads.

The SIT14503Q provides fixed output of 5V. In addition, the product family is available with fixed 2.5V, 3.3V and 15V outputs, or adjustable outputs from 0.65V to 24V [(1)]. The adjustable output voltage version uses an external resistance feedback, with a typical FB pin feedback voltage of 0.65V. The SIT14503Q can provide a load current of up to 300mA.

The power-good delay can be adjusted by external components, allowing the delay time to be configured to fit application-specific systems. When OUT reaches the PG threshold $V_{(PG-rise)}$, the Delay pin starts to output current $I_{(Charge)}$. When the Delay pin voltage reaches $V_{(RISE)}$, PG is allowed to pull up. The user can select the appropriate Delay capacitor according to the MCU delay requirements.

The SIT14503Q series features built-in protection against overcurrent, thermal shutdown and automatic restart.

NOTE [(1)]: If you need any other versions of the SIT14503Q series except for the fixed 5V output, please contact the sales.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Input voltage	VIN	-0.3	42	V
Enable voltage	EN	-0.3	VIN	V
Feedback voltage	FB	-0.3	6	V
Power good	PG	-0.3	VIN	V
Output voltage	OUT	-0.3	VIN	V
Delay	DELAY	-0.3	6	V
Ambient temperature	T_{amb}	-40	125	℃
Virtual junction temperature	T_j	-40	150	℃
Storage temperature	T_{stg}	-55	150	℃

Note: The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

DC CHARACTERISTICS

Unless otherwise stated, specified at -40℃≤T_{amb}≤125℃. Typical values are all at VIN=14V, C_{out} = 10μF, T_{amb}=25℃.

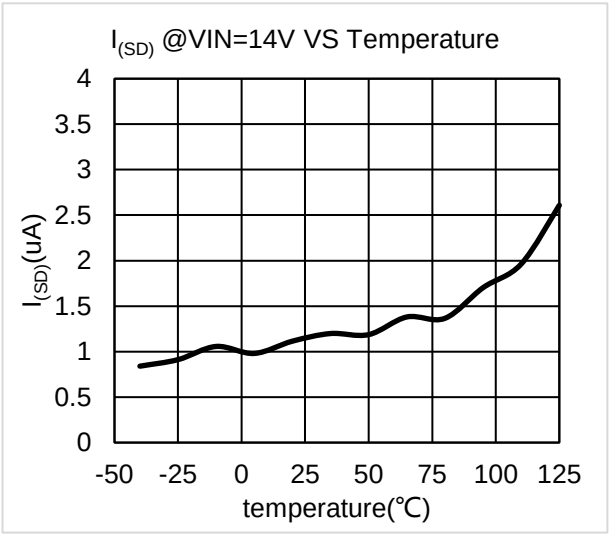
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE AND CURRENT						
V_{IN}	Input voltage		3		40	V
$I_{(SD)}$	Shutdown current	EN=0, VIN=14V		1	3	μA
$I_{(Q)}$	Quiescent current	EN=5, VIN=14V IOUT=0A		6	15	μA
ENABLE INPUT (EN)						
V_{IL}	Logic input low level				0.7	V
V_{IH}	Logic input high level		2			V
I_{EN}	EN pin input current	EN=5V		0.1	0.5	μA
REGULATED OUTPUT						
V_{OUT}	Output voltage (fixed output version)	VIN = OUT + $V_{(Dropout)}$ to 40 V, I_{OUT} = 1mA to I_{MAX}	-2		2	%
$V_{(Line-Reg)}$	Line regulation	VIN = 6 V to 40 V, I_{OUT} = 10 mA			20	mV
$V_{(Load-Reg)}$	Load regulation	VIN = 14 V, I_{OUT} = 1 mA to I_{MAX}			40	mV
DROP OUT						
$V_{(Dropout)100mA}$	Dropout voltage	OUT=5V, $I_{OUT=}$100mA		210	390	mV
$V_{(Dropout)200mA}$	Dropout voltage	OUT=5V, $I_{OUT=}$200mA		420	780	mV
$V_{(Dropout)300mA}$	Dropout voltage	OUT=5V, $I_{OUT=}$300mA		630	1170	mV
OVER CURRENT PROTECTION						
$I_{(CL)-300mA}$	Output overcurrent limit			600		mA
PSRR						
PSRR	Power supply rejection ratio	I_{OUT} =10 mA, frequency=100 Hz, C_{OUT}=2.2 μF		60 (1)		dB
THERMAL SHUTDOWN						
$T_{(SD)}$	Junction shutdown temperature			175 (1)		℃
$T_{(REC)}$	Overtemperature recovery			155 (1)		℃

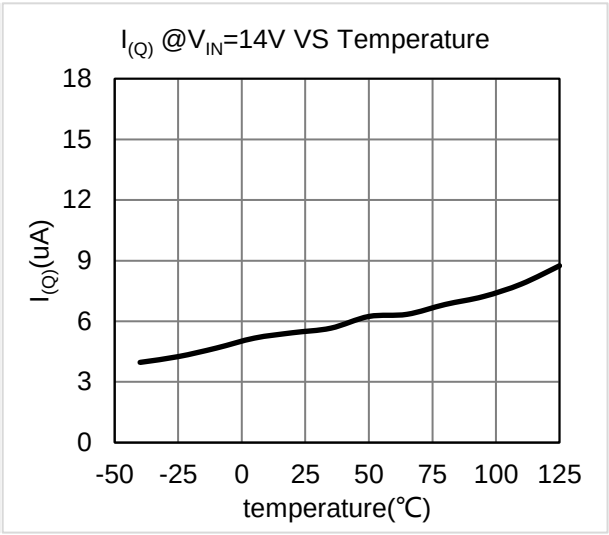
Note (1): guaranteed by designed, not tested in production.

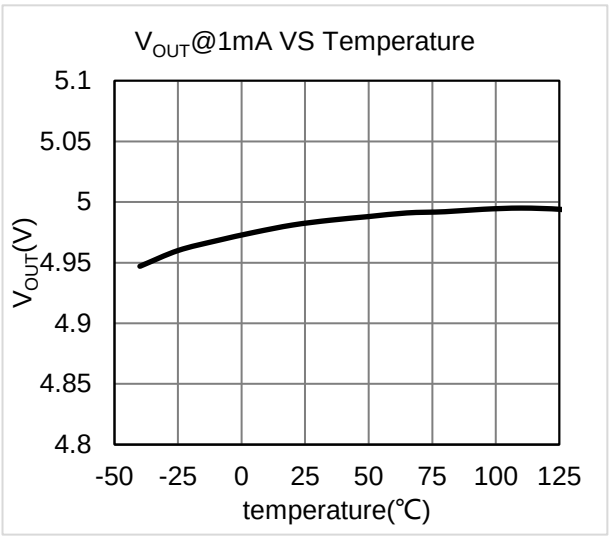
ESD PERFORMANCE

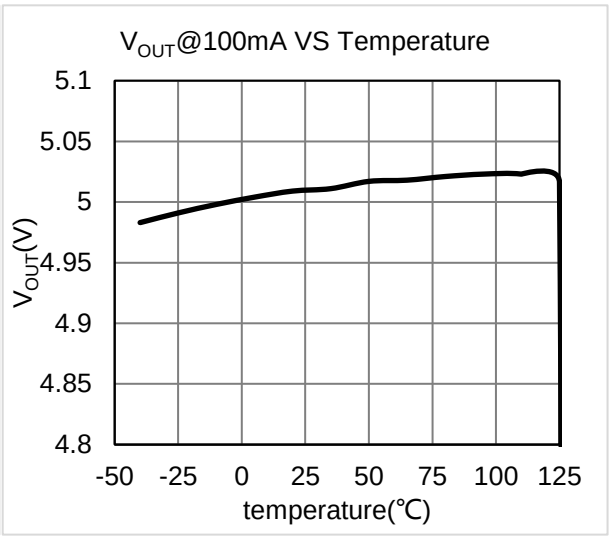
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{ESD}	HBM				±3	kV
	CDM				±750	V

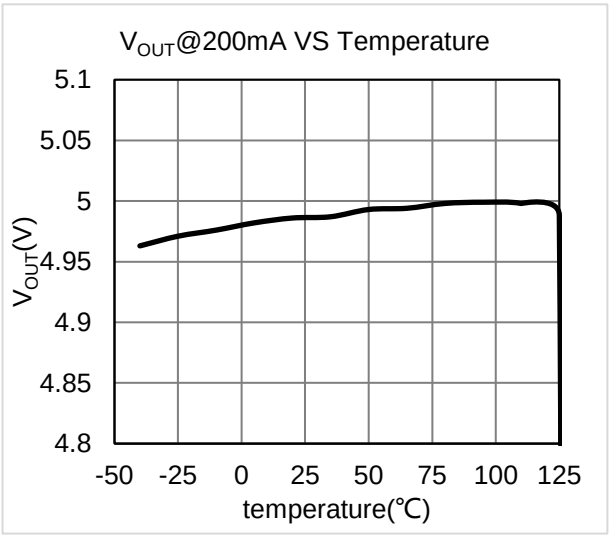
TYPICAL CHARACTERISTIC

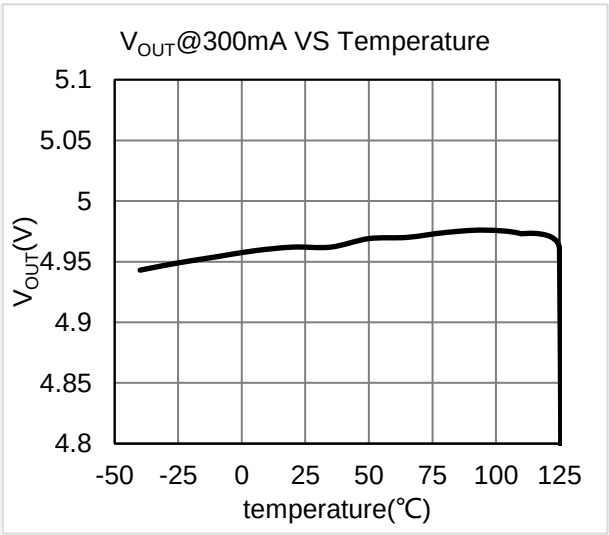


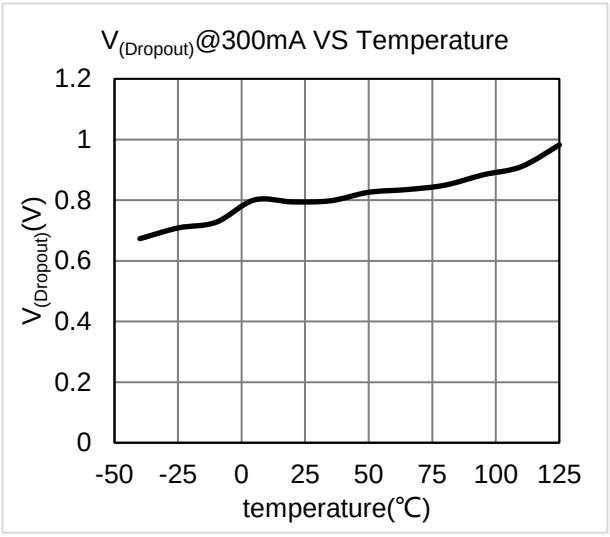


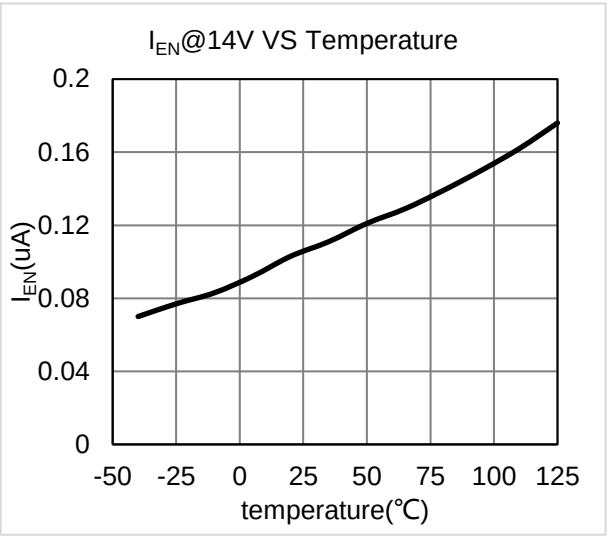


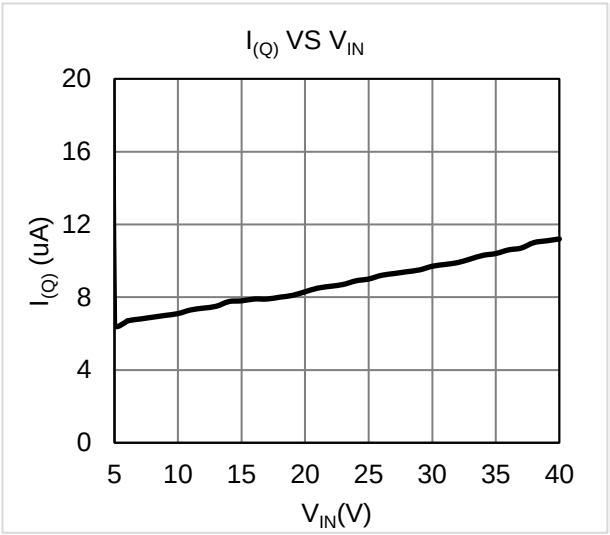


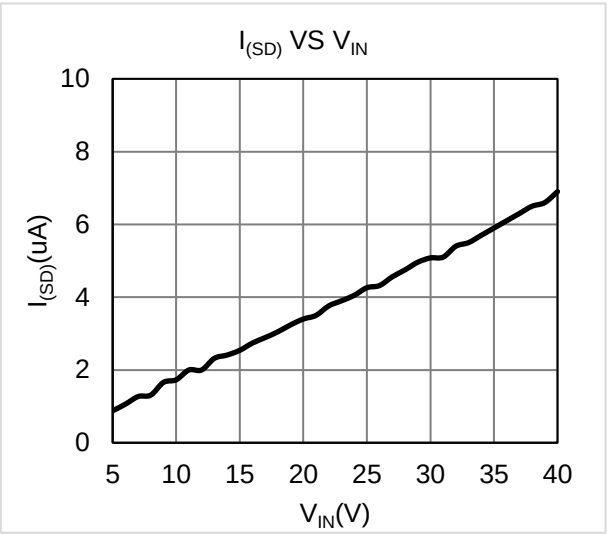


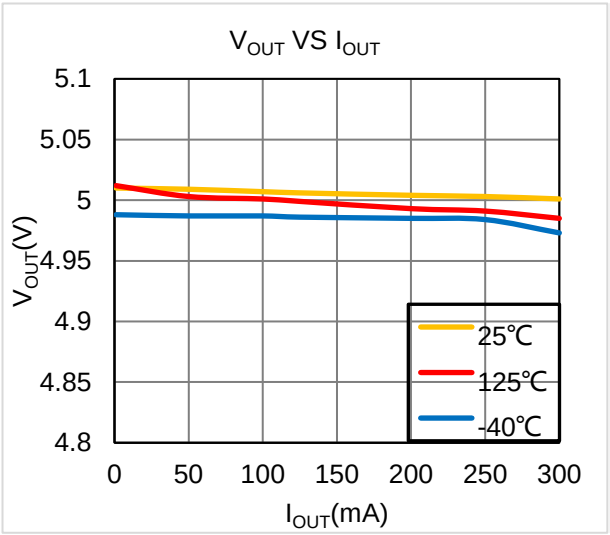


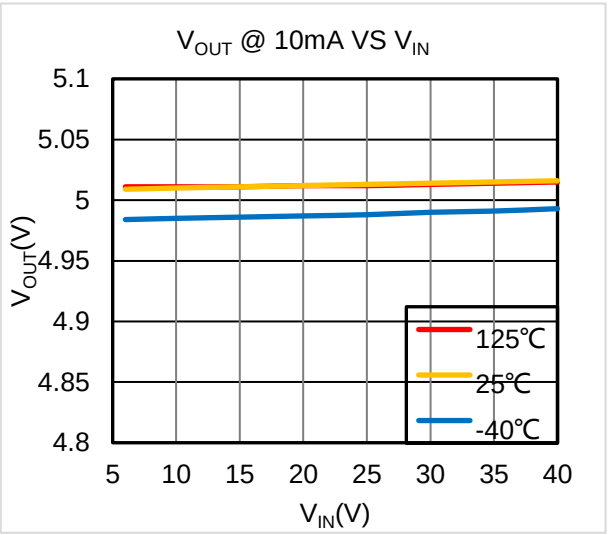

V(Dropout)@300mA VS Temperature
V(Dropout)(V)
1.2
1
0.8
0.6
0.4
0.2
0
-50 -25 0 25 50 75 100 125
temperature(℃)


IEN@14V VS Temperature
IEN(uA)
0.2
0.16
0.12
0.08
0.04
0
-50 -25 0 25 50 75 100 125
temperature(℃)

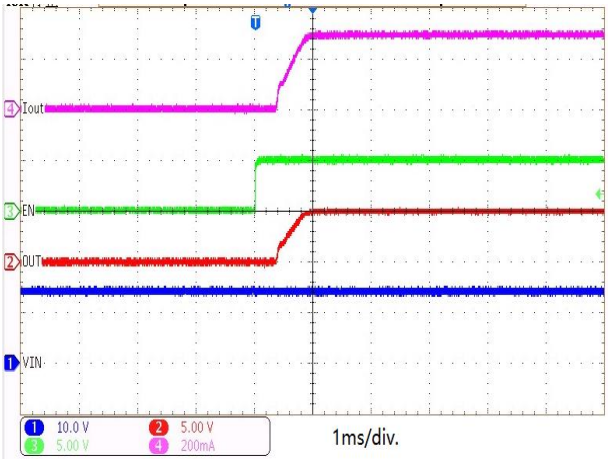

I(Q) VS VIN
I(Q) (uA)
20
16
12
8
4
0
5 10 15 20 25 30 35 40
VIN(V)


I(SD) VS VIN
I(SD)(uA)
10
8
6
4
2
0
5 10 15 20 25 30 35 40
VIN(V)

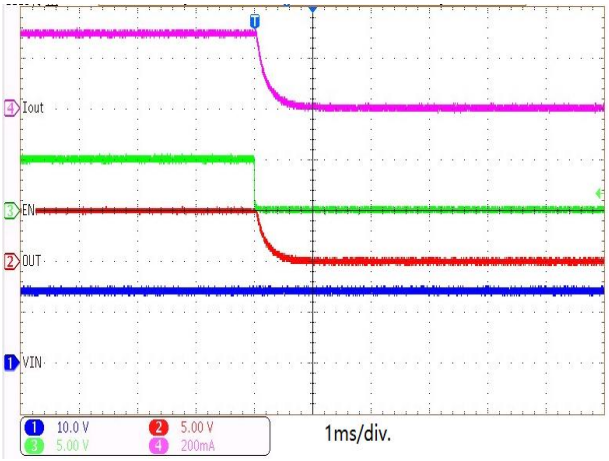

VOUT VS IOUT
VOUT(V)
5.1
5.05
5
4.95
4.9
4.85
4.8
0 50 100 150 200 250 300
IOUT(mA)
25℃
125℃
-40℃


VOUT @ 10mA VS VIN
VOUT(V)
5.1
5.05
5
4.95
4.9
4.85
4.8
5 10 15 20 25 30 35 40
VIN(V)
125℃
25℃
-40℃

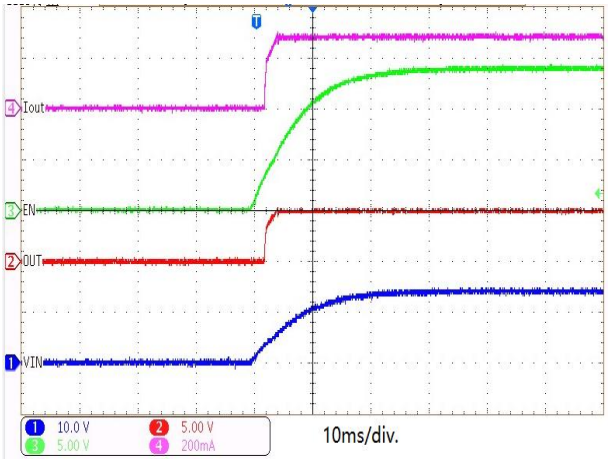
TYPICAL WAVEFORM



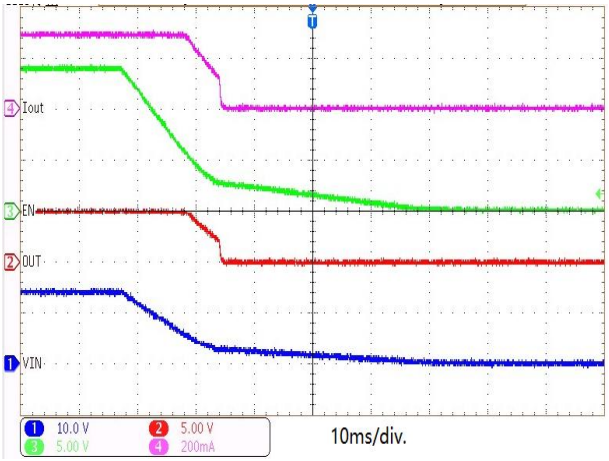
EN=L→H @ Vin=14V, Vout=5V, Rload=16Ω



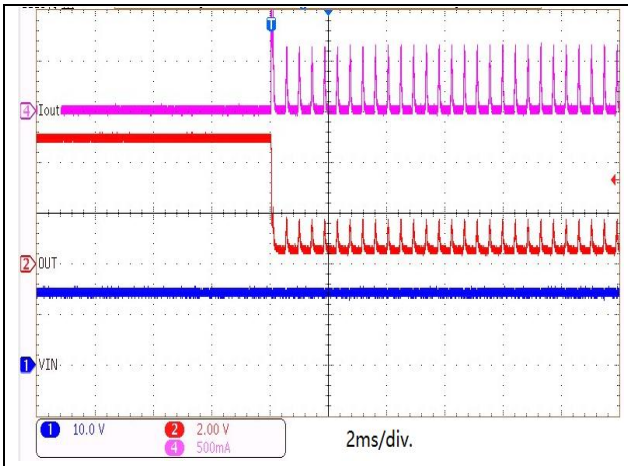
EN=H→L @ Vin=14V, Vout=5V, Rload=16Ω



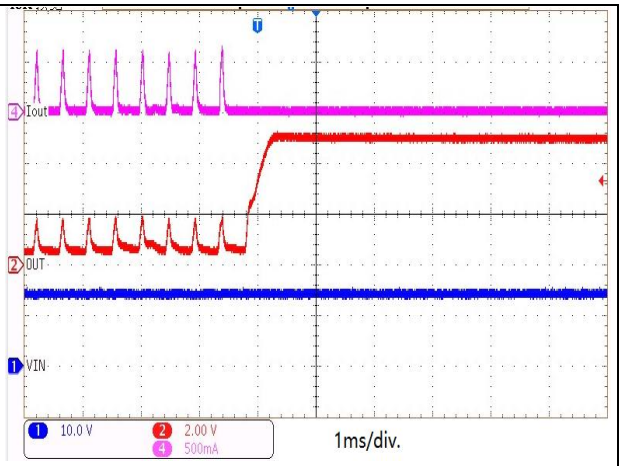
Power-Up @ Vin=VEN=14V, Vout=5V, Rload=16Ω



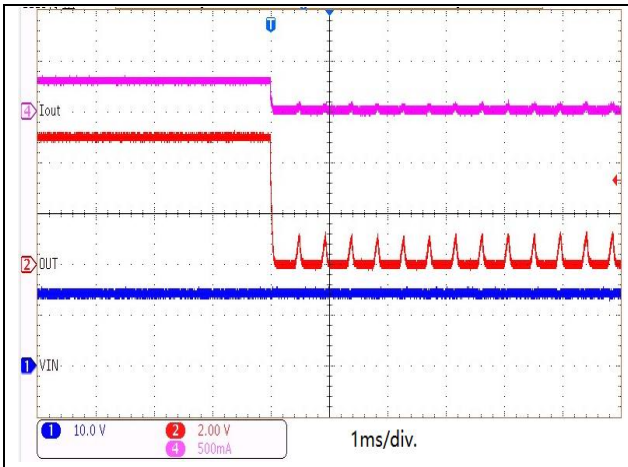
Power-OFF @ Vin=14V, Vout=5V, Rload=16Ω



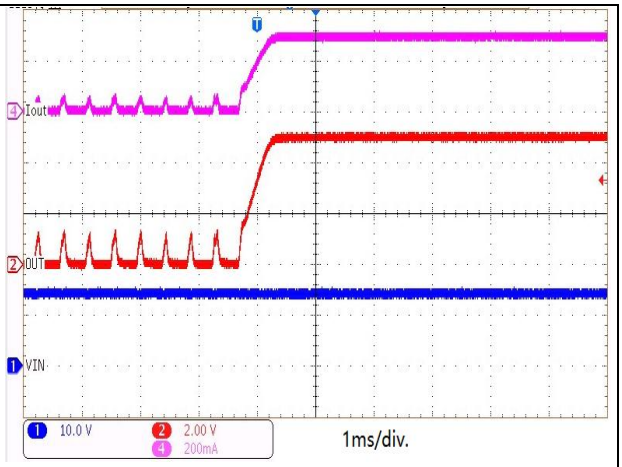
Short Circuit Entry @ no load



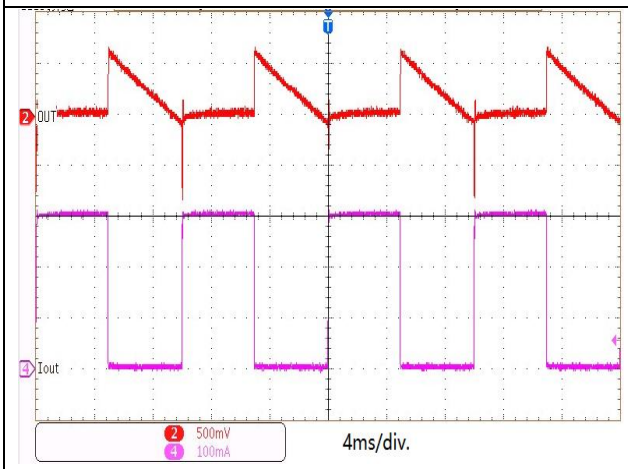
Short Circuit Recovery @ no load



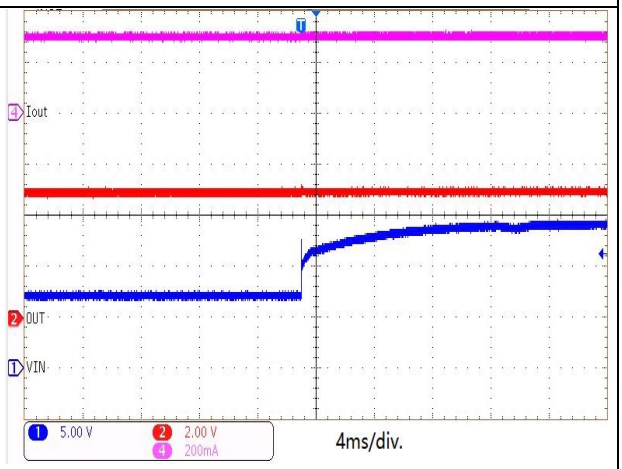
Short Circuit Entry @ Rload=16Ω



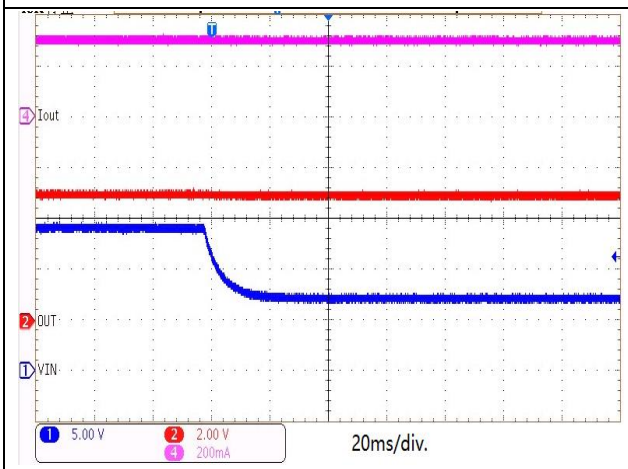
Short Circuit Recovery @ Rload=16Ω



iload =1 <-> 300mA @ Vin=14V, Vout=5V

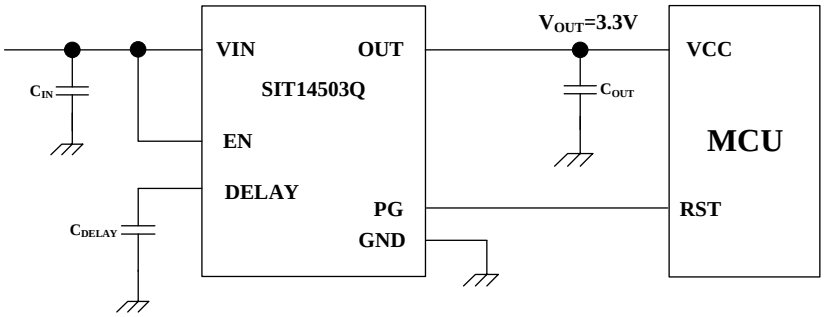


Line Transient 7 →14V vs @ Vout=5V, Rload=16Ω



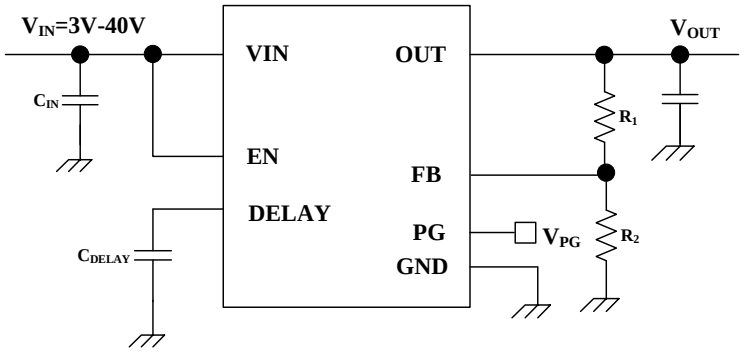
Line Transient 14V → 7V vs @ Vout=5V, Rload=16Ω

TYPICAL APPLICATION



Note: To select a capacitor for DELAY, use below equation: $C_{DELAY} = \frac{I_{(Charge)} \times t_{Delay}}{V_{(Rise)}}$

Fig 9 Typical application diagram



Note: calculate the value for V_{out} using the following equation: $V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \times V_{FB}$, it is recommended the R_2=650kΩ±1%, and the temperature coefficient is less than 100 ppm.

Fig 10 SIT14503Q/P full function application diagram

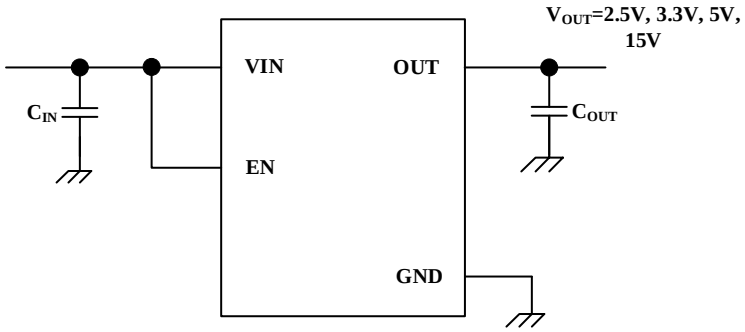
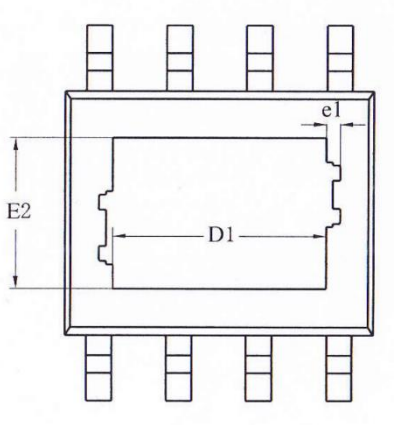


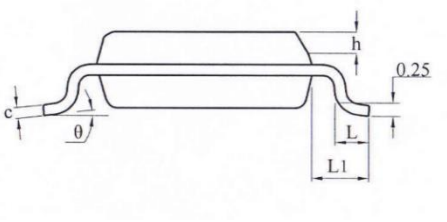
Fig 11 SIT14503Q/P simplest application diagram

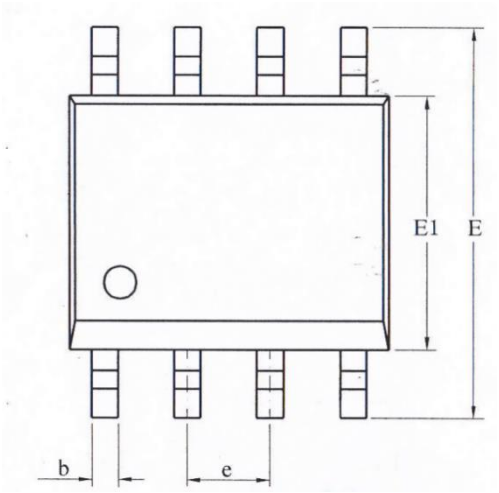
ESOP8 DIMENSION

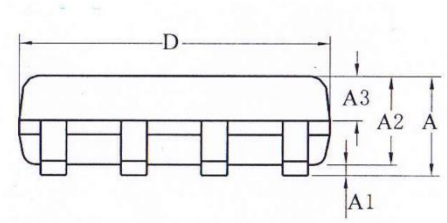
PACKAGE SIZE

Symbol	Min./mm	Typ./mm	Max./mm
A	-	-	1.65
A1	0.05	-	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
c	0.20	-	0.24
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	0.60	0.80
L1	1.05REF		
θ	0°	-	8°





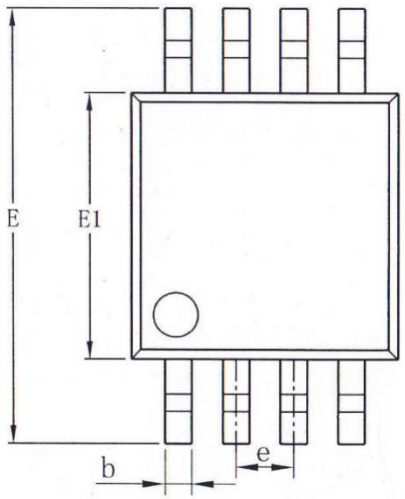


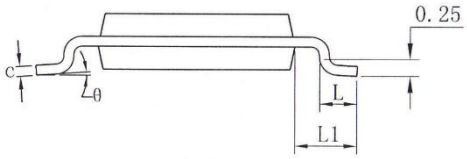


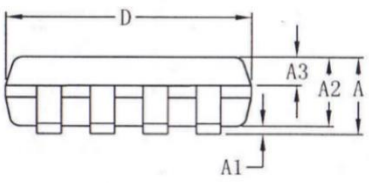
EMSOP8 DIMENSION

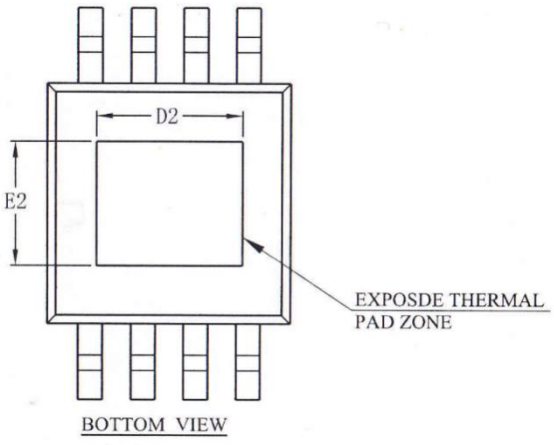
PACKAGE SIZE

Symbol	Min./mm	Typ./mm	Max./mm
A	-	-	1.10
A1	0.05	-	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	-	0.36
c	0.15	-	0.19
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65 BSC		
L	0.40	-	0.70
L1	0.95REF		
θ	0°	-	8°





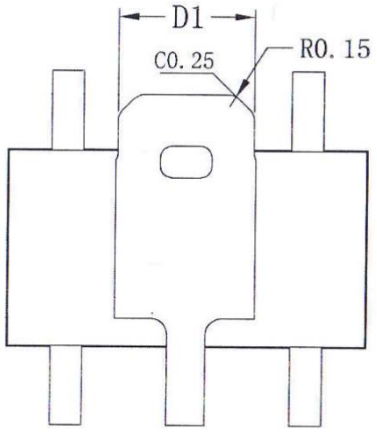


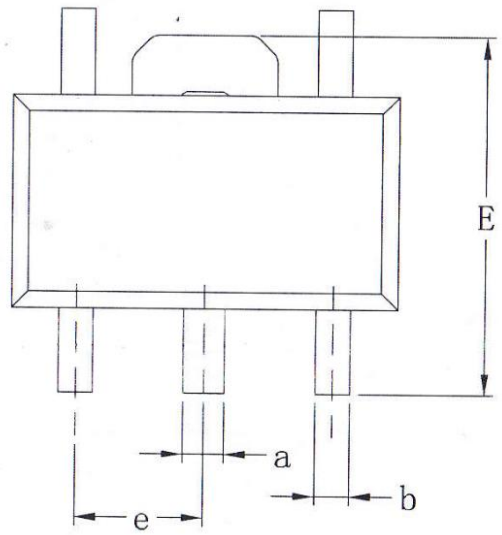


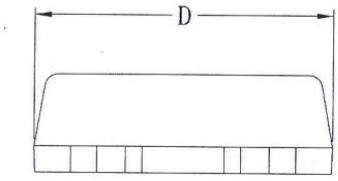
SOT89-5 DIMENSION

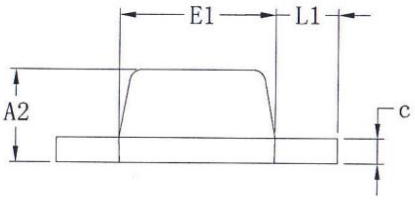
PACKAGE SIZE

Symbol	Min./mm	Typ./mm	Max./mm
A2	1.40	1.50	1.60
b	0.38	-	0.46
c	0.38	-	0.42
a	0.46	-	0.56
D	4.40	4.50	4.60
D1	1.62	-	1.83
E	3.95	3.90	4.25
E1	2.40	2.50	2.60
e	1.50BSC		
L	0.89	-	1.20
L1	1.05REF		









THERMAL INFORMATION

Symbol	Parameter	Package	Value	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	ESOP8	42	℃/W
		EMSOP8	67	℃/W
		SOT89-5	50	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	ESOP8	8	℃/W
		EMSOP	40	℃/W
		SOT89-5	44	℃/W

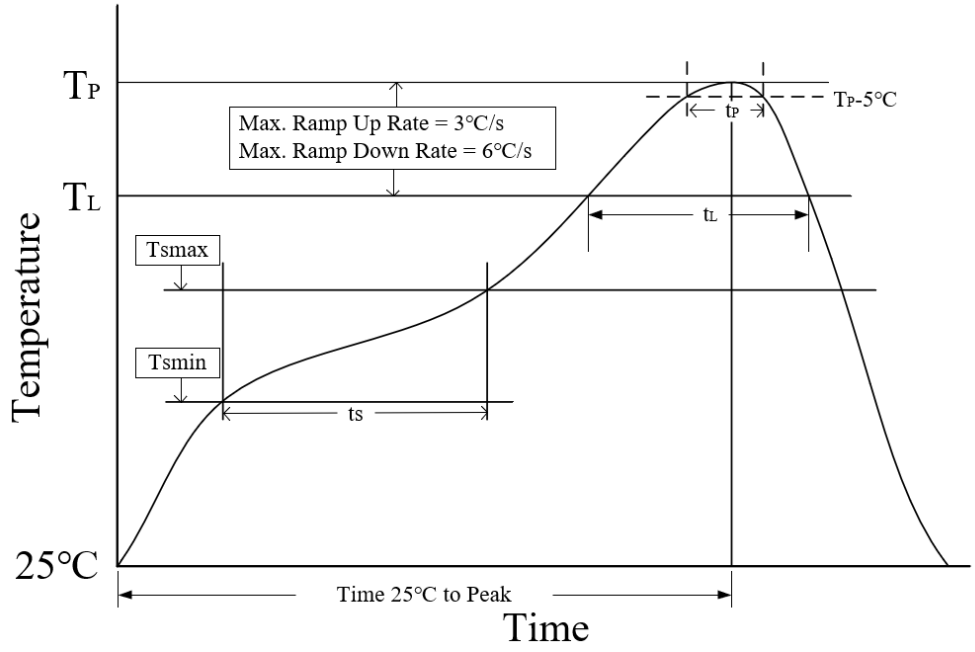
Note: According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board.

ORDERING INFORMATION

Type number	Output voltage	Output current	PG function	Package	Packing
SIT14503QT/P	5V	300mA	√	ESOP8	Tape and reel
SIT14503QU	5V	300mA	×	EMSOP8	Tape and reel
SIT14503QS	5V	300mA	×	SOT89-5	Tape and reel

2500 pieces/disc in taped packages.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150°C to T_{smax}=200°C)	60-120 seconds
Melting time t_L (T_L=217°C)	60-150 seconds
Peak temp T_P	260-265 °C
5°C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°C to peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Data sheet status	Revision date
V1.0	Initial version.	September 2023